

# MC74LCX573

## Low-Voltage CMOS Octal Transparent Latch Flow Through Pinout

### With 5 V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

The MC74LCX573 is a high performance, non-inverting octal transparent latch operating from a 2.3 to 3.6 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A  $V_I$  specification of 5.5 V allows MC74LCX573 inputs to be safely driven from 5.0 V devices.

The MC74LCX573 contains 8 D-type latches with 3-state standard outputs. When the Latch Enable (LE) input is HIGH, data on the Dn inputs enters the latches. In this condition, the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state standard outputs are controlled by the Output Enable ( $\overline{OE}$ ) input. When  $\overline{OE}$  is LOW, the standard outputs are enabled. When  $\overline{OE}$  is HIGH, the standard outputs are in the high impedance state, but this does not interfere with new data entering into the latches. The LCX573 flow through design facilitates easy PC board layout.

#### Features

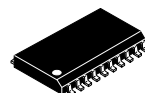
- Designed for 2.3 to 3.6 V  $V_{CC}$  Operation
- 5.0 V Tolerant – Interface Capability With 5.0 V TTL Logic
- Supports Live Insertion and Withdrawal
- $I_{OFF}$  Specification Guarantees High Impedance When  $V_{CC} = 0$  V
- LVTTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10  $\mu$ A)  
Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500 mA
- ESD Performance:
  - ♦ Human Body Model >2000 V
  - ♦ Machine Model >200 V
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



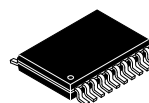
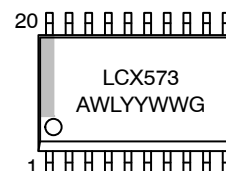
ON Semiconductor®

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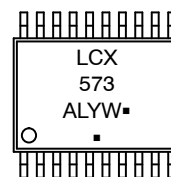
#### MARKING DIAGRAMS



SOIC-20 WB  
DW SUFFIX  
CASE 751D



TSSOP-20  
DT SUFFIX  
CASE 948E



A = Assembly Location  
L, WL = Wafer Lot  
Y, YY = Year  
W, WW = Work Week  
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

MC74LCX573

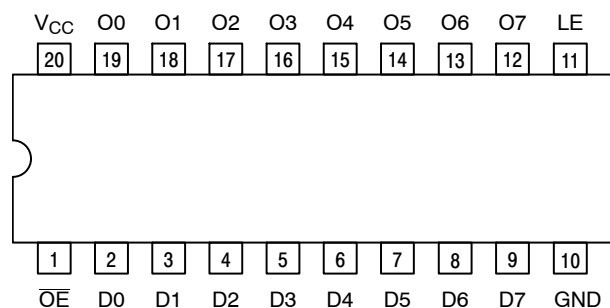


Figure 1. Pinout (Top View)

PIN NAMES

| Pins  | Function              |
|-------|-----------------------|
| OE    | Output Enable Input   |
| LE    | Latch Enable Input    |
| D0–D7 | Data Inputs           |
| O0–O7 | 3–State Latch Outputs |

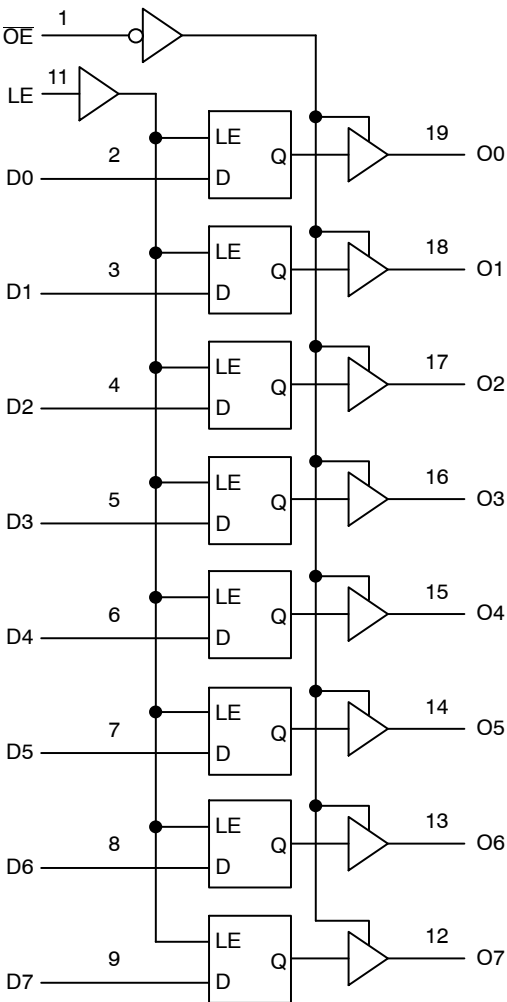


Figure 2. Logic Diagram

TRUTH TABLE

| Inputs |    |    | Outputs | Operating Mode                                 |
|--------|----|----|---------|------------------------------------------------|
| OE     | LE | Dn | On      |                                                |
| L      | H  | H  | H       | Transparent (Latch Disabled); Read Latch       |
| L      | H  | L  | L       |                                                |
| L      | L  | h  | H       | Latched (Latch Enabled) Read Latch             |
| L      | L  | L  | L       |                                                |
| L      | L  | X  | NC      | Hold; Read Latch                               |
| H      | L  | X  | Z       | Hold; Disabled Outputs                         |
| H      | H  | H  | Z       | Transparent (Latch Disabled); Disabled Outputs |
| H      | H  | L  | Z       |                                                |
| H      | L  | h  | Z       | Latched (Latch Enabled); Disabled Outputs      |
| H      | L  | L  | Z       |                                                |

H = High Voltage Level;  
h = High Voltage Level One Setup Time Prior to the Latch Enable High-to-Low Transition  
L = Low Voltage Level  
l = Low Voltage Level One Setup Time Prior to the Latch Enable High-to-Low Transition  
NC = No Change, State Prior to the Latch Enable High-to-Low Transition  
X = High or Low Voltage Level or Transitions are Acceptable  
Z = High Impedance State  
For I<sub>CC</sub> Reasons DO NOT FLOAT Inputs

# MC74LCX573

## MAXIMUM RATINGS

| Symbol    | Parameter                        | Value                             | Condition                            | Units |
|-----------|----------------------------------|-----------------------------------|--------------------------------------|-------|
| $V_{CC}$  | DC Supply Voltage                | -0.5 to +7.0                      |                                      | V     |
| $V_I$     | DC Input Voltage                 | $-0.5 \leq V_I \leq +7.0$         |                                      | V     |
| $V_O$     | DC Output Voltage                | $-0.5 \leq V_O \leq +7.0$         | Output in 3-State                    | V     |
|           |                                  | $-0.5 \leq V_O \leq V_{CC} + 0.5$ | Output in HIGH or LOW State (Note 1) | V     |
| $I_{IK}$  | DC Input Diode Current           | -50                               | $V_I < GND$                          | mA    |
| $I_{OK}$  | DC Output Diode Current          | -50                               | $V_O < GND$                          | mA    |
|           |                                  | +50                               | $V_O > V_{CC}$                       | mA    |
| $I_O$     | DC Output Source/Sink Current    | $\pm 50$                          |                                      | mA    |
| $I_{CC}$  | DC Supply Current Per Supply Pin | $\pm 100$                         |                                      | mA    |
| $I_{GND}$ | DC Ground Current Per Ground Pin | $\pm 100$                         |                                      | mA    |
| $T_{STG}$ | Storage Temperature Range        | -65 to +150                       |                                      | °C    |
| MSL       | Moisture Sensitivity             |                                   | Level 1                              |       |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1.  $I_O$  absolute maximum rating must be observed.

## RECOMMENDED OPERATING CONDITIONS

| Symbol              | Parameter                                                                                                                                               | Min        | Typ                  | Max              | Units |
|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|------------|----------------------|------------------|-------|
| $V_{CC}$            | Supply Voltage<br>Operating<br>Data Retention Only                                                                                                      | 2.0<br>1.5 | 2.5, 3.3<br>2.5, 3.3 | 3.6<br>3.6       | V     |
| $V_I$               | Input Voltage                                                                                                                                           | 0          |                      | 5.5              | V     |
| $V_O$               | Output Voltage<br>(HIGH or LOW State)<br>(3-State)                                                                                                      | 0<br>0     |                      | $V_{CC}$<br>5.5  | V     |
| $I_{OH}$            | HIGH Level Output Current<br>$V_{CC} = 3.0\text{ V} - 3.6\text{ V}$<br>$V_{CC} = 2.7\text{ V} - 3.0\text{ V}$<br>$V_{CC} = 2.3\text{ V} - 2.7\text{ V}$ |            |                      | -24<br>-12<br>-8 | mA    |
| $I_{OL}$            | LOW Level Output Current<br>$V_{CC} = 3.0\text{ V} - 3.6\text{ V}$<br>$V_{CC} = 2.7\text{ V} - 3.0\text{ V}$<br>$V_{CC} = 2.3\text{ V} - 2.7\text{ V}$  |            |                      | +24<br>+12<br>+8 | mA    |
| $T_A$               | Operating Free-Air Temperature                                                                                                                          | -55        |                      | +125             | °C    |
| $\Delta t/\Delta V$ | Input Transition Rise or Fall Rate, $V_{IN}$ from 0.8 V to 2.0 V, $V_{CC} = 3.0\text{ V}$                                                               | 0          |                      | 10               | ns/V  |

## ORDERING INFORMATION

| Device            | Package               | Shipping†        |
|-------------------|-----------------------|------------------|
| MC74LCX573DWG     | SOIC-20<br>(Pb-Free)  | 38 Units / Rail  |
| MC74LCX573DWR2G   | SOIC-20<br>(Pb-Free)  | 1000 Tape & Reel |
| MC74LCX573DTG     | TSSOP-20<br>(Pb-Free) | 75 Units / Rail  |
| MC74LCX573DTR2G   | TSSOP-20<br>(Pb-Free) | 2500 Tape & Reel |
| NLV74LCX573DTR2G* | TSSOP-20<br>(Pb-Free) | 2500 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

## DC ELECTRICAL CHARACTERISTICS

| Symbol           | Characteristic                        | Condition                                                                                                     | T <sub>A</sub> = -40°C to +85°C |      | T <sub>A</sub> = -55°C to +125°C |      | Units |
|------------------|---------------------------------------|---------------------------------------------------------------------------------------------------------------|---------------------------------|------|----------------------------------|------|-------|
|                  |                                       |                                                                                                               | Min                             | Max  | Min                              | Max  |       |
| V <sub>IH</sub>  | HIGH Level Input Voltage (Note 2)     | 2.3 V ≤ V <sub>CC</sub> ≤ 2.7 V                                                                               | 1.7                             |      | 1.7                              |      | V     |
|                  |                                       | 2.7 V ≤ V <sub>CC</sub> ≤ 3.6 V                                                                               | 2.0                             |      | 2.0                              |      |       |
| V <sub>IL</sub>  | LOW Level Input Voltage (Note 2)      | 2.3 V ≤ V <sub>CC</sub> ≤ 2.7 V                                                                               |                                 | 0.7  |                                  | 0.7  | V     |
|                  |                                       | 2.7 V ≤ V <sub>CC</sub> ≤ 3.6 V                                                                               |                                 | 0.8  |                                  | 0.8  |       |
| V <sub>OH</sub>  | HIGH Level Output Voltage             | 2.3 V ≤ V <sub>CC</sub> ≤ 3.6 V; I <sub>OL</sub> = 100 μA                                                     | V <sub>CC</sub> - 0.2           |      | V <sub>CC</sub> - 0.2            |      | V     |
|                  |                                       | V <sub>CC</sub> = 2.3 V; I <sub>OH</sub> = -8 mA                                                              | 1.8                             |      | 1.8                              |      |       |
|                  |                                       | V <sub>CC</sub> = 2.7 V; I <sub>OH</sub> = -12 mA                                                             | 2.2                             |      | 2.2                              |      |       |
|                  |                                       | V <sub>CC</sub> = 3.0 V; I <sub>OH</sub> = -18 mA                                                             | 2.4                             |      | 2.4                              |      |       |
|                  |                                       | V <sub>CC</sub> = 3.0 V; I <sub>OH</sub> = -24 mA                                                             | 2.2                             |      | 2.2                              |      |       |
| V <sub>OL</sub>  | LOW Level Output Voltage              | 2.3 V ≤ V <sub>CC</sub> ≤ 3.6 V; I <sub>OL</sub> = 100 μA                                                     |                                 | 0.2  |                                  | 0.2  | V     |
|                  |                                       | V <sub>CC</sub> = 2.3 V; I <sub>OL</sub> = 8 mA                                                               |                                 | 0.6  |                                  | 0.6  |       |
|                  |                                       | V <sub>CC</sub> = 2.7 V; I <sub>OL</sub> = 12 mA                                                              |                                 | 0.4  |                                  | 0.4  |       |
|                  |                                       | V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 16 mA                                                              |                                 | 0.4  |                                  | 0.4  |       |
|                  |                                       | V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 24 mA                                                              |                                 | 0.55 |                                  | 0.60 |       |
| I <sub>OZ</sub>  | 3-State Output Current                | V <sub>CC</sub> = 3.6 V, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> = 0 to 5.5 V |                                 | ±5   |                                  | ±5   | μA    |
| I <sub>OFF</sub> | Power Off Leakage Current             | V <sub>CC</sub> = 0, V <sub>IN</sub> = 5.5 V or V <sub>OUT</sub> = 5.5 V                                      |                                 | 10   |                                  | 10   | μA    |
| I <sub>IN</sub>  | Input Leakage Current                 | V <sub>CC</sub> = 3.6 V, V <sub>IN</sub> = 5.5 V or GND                                                       |                                 | ±5   |                                  | ±5   | μA    |
| I <sub>CC</sub>  | Quiescent Supply Current              | V <sub>CC</sub> = 3.6 V, V <sub>IN</sub> = 5.5 V or GND                                                       |                                 | 10   |                                  | 10   | μA    |
| ΔI <sub>CC</sub> | Increase in I <sub>CC</sub> per Input | 2.3 ≤ V <sub>CC</sub> ≤ 3.6 V; V <sub>IH</sub> = V <sub>CC</sub> - 0.6 V                                      |                                 | 500  |                                  | 500  | μA    |

2. These values of V<sub>I</sub> are used to test DC electrical characteristics only.

AC CHARACTERISTICS t<sub>R</sub> = t<sub>F</sub> = 2.5 ns; R<sub>L</sub> = 500 Ω

| Symbol                                 | Parameter                                             | Waveform | Limits                           |            |                         |            |                                 |              | Units |
|----------------------------------------|-------------------------------------------------------|----------|----------------------------------|------------|-------------------------|------------|---------------------------------|--------------|-------|
|                                        |                                                       |          | T <sub>A</sub> = -55°C to +125°C |            |                         |            |                                 |              |       |
|                                        |                                                       |          | V <sub>CC</sub> = 3.3 V ± 0.3 V  |            | V <sub>CC</sub> = 2.7 V |            | V <sub>CC</sub> = 2.5 V ± 0.2 V |              |       |
|                                        |                                                       |          | C <sub>L</sub> = 50 pF           |            | C <sub>L</sub> = 50 pF  |            | C <sub>L</sub> = 30 pF          |              |       |
|                                        |                                                       |          | Min                              | Max        | Min                     | Max        | Min                             | Max          |       |
| t <sub>PLH</sub><br>t <sub>PHL</sub>   | Propagation Delay<br>D <sub>n</sub> to O <sub>n</sub> | 1        | 1.5<br>1.5                       | 8.0<br>8.0 | 1.5<br>1.5              | 9.0<br>9.0 | 1.5<br>1.5                      | 9.6<br>9.6   | ns    |
| t <sub>PLH</sub><br>t <sub>PHL</sub>   | Propagation Delay<br>LE to O <sub>n</sub>             | 3        | 1.5<br>1.5                       | 8.5<br>8.5 | 1.5<br>1.5              | 9.5<br>9.5 | 1.5<br>1.5                      | 10.5<br>10.5 | ns    |
| t <sub>PZH</sub><br>t <sub>PZL</sub>   | Output Enable Time to HIGH<br>and LOW Level           | 2        | 1.5<br>1.5                       | 8.5<br>8.5 | 1.5<br>1.5              | 9.5<br>9.5 | 1.5<br>1.5                      | 10.5<br>10.5 | ns    |
| t <sub>PHZ</sub><br>t <sub>PLZ</sub>   | Output Disable Time From<br>High and Low Level        | 2        | 1.5<br>1.5                       | 6.5<br>6.5 | 1.5<br>1.5              | 7.0<br>7.0 | 1.5<br>1.5                      | 7.8<br>7.8   | ns    |
| t <sub>s</sub>                         | Setup Time, HIGH or LOW<br>D <sub>n</sub> to LE       | 3        | 2.5                              |            | 2.5                     |            | 4.0                             |              |       |
| t <sub>h</sub>                         | Hold Time, HIGH or LOW<br>D <sub>n</sub> to LE        | 3        | 1.5                              |            | 1.5                     |            | 2.0                             |              |       |
| t <sub>w</sub>                         | LE Pulse Width, HIGH                                  | 3        | 3.3                              |            | 3.3                     |            | 4.0                             |              |       |
| t <sub>OSHL</sub><br>t <sub>OSLH</sub> | Output-to-Output Skew<br>(Note 3)                     |          |                                  | 1.0<br>1.0 |                         |            |                                 |              | ns    |

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>); parameter guaranteed by design.

# MC74LCX573

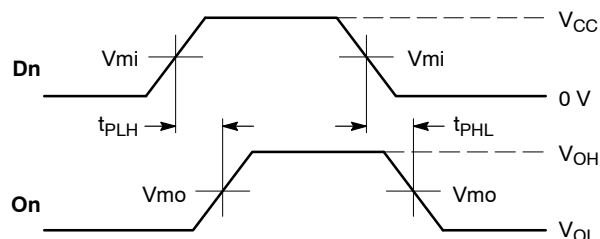
## DYNAMIC SWITCHING CHARACTERISTICS

| Symbol    | Characteristic                         | Condition                                                                                                                                                                          | $T_A = +25^\circ\text{C}$ |              |     | Units  |
|-----------|----------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|--------------|-----|--------|
|           |                                        |                                                                                                                                                                                    | Min                       | Typ          | Max |        |
| $V_{OLP}$ | Dynamic LOW Peak Voltage<br>(Note 4)   | $V_{CC} = 3.3\text{ V}, C_L = 50\text{ pF}, V_{IH} = 3.3\text{ V}, V_{IL} = 0\text{ V}$<br>$V_{CC} = 2.5\text{ V}, C_L = 30\text{ pF}, V_{IH} = 2.5\text{ V}, V_{IL} = 0\text{ V}$ |                           | 0.8<br>0.6   |     | V<br>V |
| $V_{OLV}$ | Dynamic LOW Valley Voltage<br>(Note 4) | $V_{CC} = 3.3\text{ V}, C_L = 50\text{ pF}, V_{IH} = 3.3\text{ V}, V_{IL} = 0\text{ V}$<br>$V_{CC} = 2.5\text{ V}, C_L = 30\text{ pF}, V_{IH} = 2.5\text{ V}, V_{IL} = 0\text{ V}$ |                           | -0.8<br>-0.6 |     | V<br>V |

4. Number of outputs defined as “n”. Measured with “n-1” outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

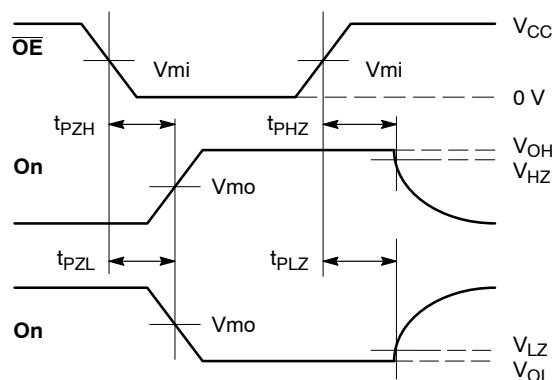
## CAPACITIVE CHARACTERISTICS

| Symbol    | Parameter                     | Condition                                                    | Typical | Units |
|-----------|-------------------------------|--------------------------------------------------------------|---------|-------|
| $C_{IN}$  | Input Capacitance             | $V_{CC} = 3.3\text{ V}, V_I = 0\text{ V or } V_{CC}$         | 7       | pF    |
| $C_{I/O}$ | Input/Output Capacitance      | $V_{CC} = 3.3\text{ V}, V_I = 0\text{ V or } V_{CC}$         | 8       | pF    |
| $C_{PD}$  | Power Dissipation Capacitance | 10 MHz, $V_{CC} = 3.3\text{ V}, V_I = 0\text{ V or } V_{CC}$ | 25      | pF    |



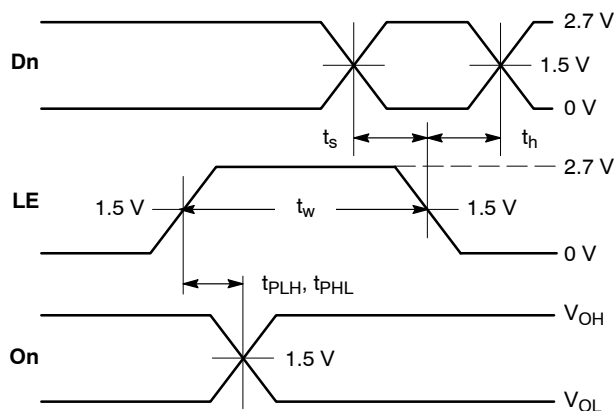
**WAVEFORM 1 – PROPAGATION DELAYS**

$t_R = t_F = 2.5\text{ ns}$ , 10% to 90%;  $f = 1\text{ MHz}$ ;  $t_W = 500\text{ ns}$



**WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES**

$t_R = t_F = 2.5\text{ ns}$ , 10% to 90%;  $f = 1\text{ MHz}$ ;  $t_W = 500\text{ ns}$



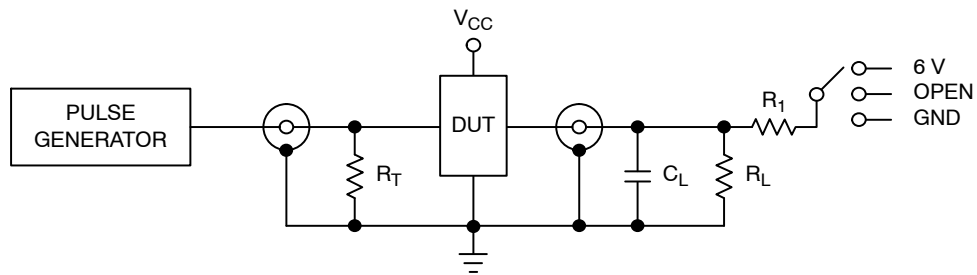
**WAVEFORM 3 – LE to On PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, Dn to LE SETUP AND HOLD TIMES**

$t_R = t_F = 2.5\text{ ns}$ , 10% to 90%;  $f = 1\text{ MHz}$ ;  $t_W = 500\text{ ns}$  except when noted

| Symbol   | $V_{CC}$                        |                         |                                 |
|----------|---------------------------------|-------------------------|---------------------------------|
|          | $3.3\text{ V} \pm 0.3\text{ V}$ | $2.7\text{ V}$          | $2.5\text{ V} \pm 0.2\text{ V}$ |
| $V_{mi}$ | 1.5 V                           | 1.5 V                   | $V_{CC}/2$                      |
| $V_{mo}$ | 1.5 V                           | 1.5 V                   | $V_{CC}/2$                      |
| $V_{HZ}$ | $V_{OL} + 0.3\text{ V}$         | $V_{OL} + 0.3\text{ V}$ | $V_{OL} + 0.15\text{ V}$        |
| $V_{LZ}$ | $V_{OL} - 0.3\text{ V}$         | $V_{OL} - 0.3\text{ V}$ | $V_{OL} - 0.15\text{ V}$        |

**Figure 3. AC Waveforms**

## MC74LCX573



| Test                                         | Switch                                                             |
|----------------------------------------------|--------------------------------------------------------------------|
| $t_{PLH}$ , $t_{PHL}$                        | Open                                                               |
| $t_{PZL}$ , $t_{PLZ}$                        | 6 V at $V_{CC} = 3.3 \pm 0.3$ V<br>6 V at $V_{CC} = 2.5 \pm 0.2$ V |
| Open Collector/Drain $t_{PLH}$ and $t_{PHL}$ | 6 V                                                                |
| $t_{PZH}$ , $t_{PHZ}$                        | GND                                                                |

$C_L = 50$  pF at  $V_{CC} = 3.3 \pm 0.3$  V or equivalent (includes jig and probe capacitance)

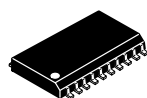
$C_L = 30$  pF at  $V_{CC} = 2.5 \pm 0.2$  V or equivalent (includes jig and probe capacitance)

$R_L = R_1 = 500 \Omega$  or equivalent

$R_T = Z_{OUT}$  of pulse generator (typically  $50 \Omega$ )

**Figure 4. Test Circuit**

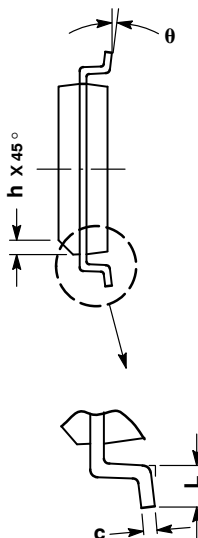
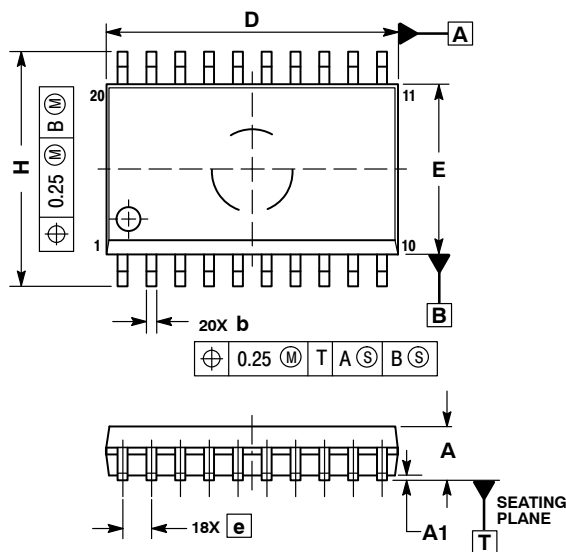
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-20 WB  
CASE 751D-05  
ISSUE H

DATE 22 APR 2015

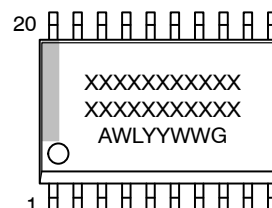


## NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

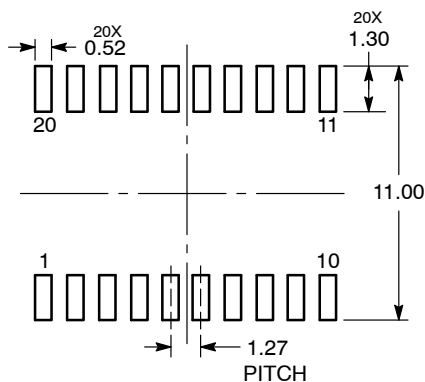
| DIM | MILLIMETERS |       |
|-----|-------------|-------|
|     | MIN         | MAX   |
| A   | 2.35        | 2.65  |
| A1  | 0.10        | 0.25  |
| b   | 0.35        | 0.49  |
| c   | 0.23        | 0.32  |
| D   | 12.65       | 12.95 |
| E   | 7.40        | 7.60  |
| e   | 1.27 BSC    |       |
| H   | 10.05       | 10.55 |
| h   | 0.25        | 0.75  |
| L   | 0.50        | 0.90  |
| θ   | 0°          | 7°    |

## GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

## RECOMMENDED SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

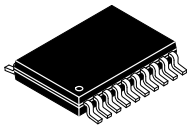
|                  |             |                                                                                                                                                                                     |
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| DESCRIPTION:     | SOIC-20 WB  | PAGE 1 OF 1                                                                                                                                                                         |

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

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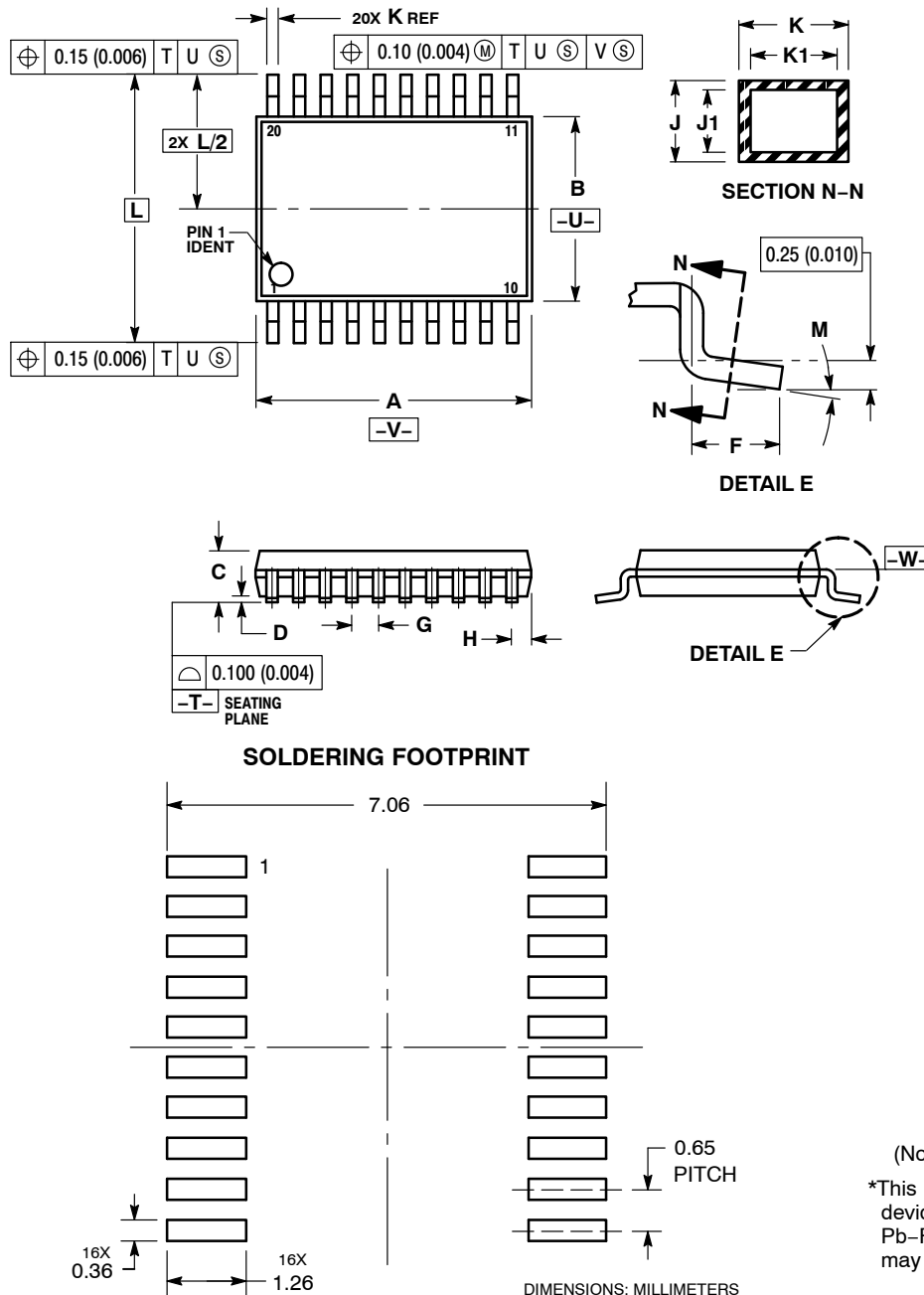
ON



SCALE 2:1

TSSOP-20 WB  
CASE 948E  
ISSUE D

DATE 17 FEB 2016

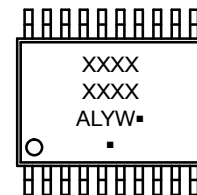


## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 6.40        | 6.60 | 0.252     | 0.260 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.27        | 0.37 | 0.011     | 0.015 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

## GENERIC MARKING DIAGRAM\*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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DESCRIPTION: TSSOP-20 WB

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